Features

Input and output interface capability to systems at 5V V_{CC}

Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH162245), also available without bushold feature (74LVT162245).

Live insertion/extraction permitted

Power Up/Down high impedance provides glitch-free bus loading

A Port outputs include equivalent series resistance of 25: making external termination resistors unnecessary and reducing overshoot and undershoot

A Port outputs source/sink r

Logic Symbol

Connection Diagrams

Pin Assignments for SSOP and TSSOP
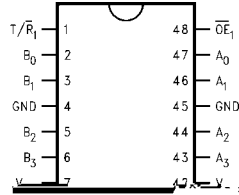
Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs/3-STATE Outputs
B_0–B_{15}	Side B Inputs 3-STATE Outputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	B_0	NC	$T/\overline{R}_1$	$\overline{OE}_1$	NC	A_0
B	B_2	B_1	NC	NC	A_1	A_2
C	B_4	B_3	V_{CC}	V_{CC}	A_3	A_4
D	B_6	B_5	GND	GND	A_5	A_6
E	B_8	B_7	GND	GND	A_7	A_8
F	B_{10}	B_9	GND	GND	A_9	A_{10}
G	B_{12}	B_{11}	V_{CC}	V_{CC}	A_{11}	A_{12}
H	B_{14}	B_{13}	NC	NC	A_{13}	A_{14}
J	B_{15}	NC	$T/\overline{R}_2$	$\overline{OE}_2$	NC	A_{15}

Pin Assignment for FBGA

(Top Thru View)

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH-Z State on A_0–A_7, B_0–B_7

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH-Z State on A_8–A_{15}, B_8–B_{15}

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
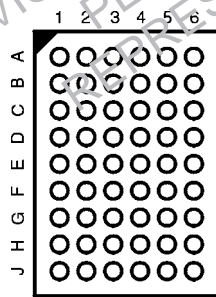
Functional Description

The LVT162245 and LVTH162245 contain sixteen non-inverting bidirectional buffers with 3-STATE outputs. The device is byte controlled with each byte functioning identi-cally, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Logic Diagrams
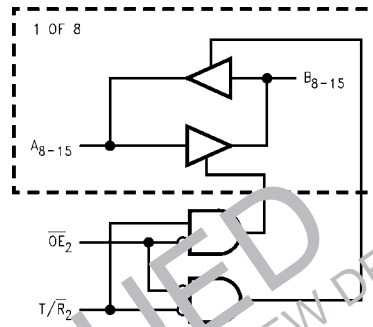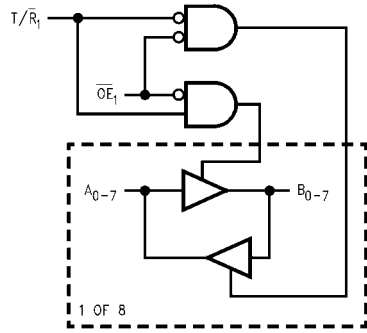
Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings   (Note 3)

Recommended Operating Conditions

Note 3: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_CC (V)	T_A = −40°C to +85°C		Units	Conditions
			Min	Max		
$I_{PU/PD}$	Power Up/Down 3-STATE Current	0–1.5V		±100	μA	V_O = 0.5V to 3.0V V_I = GND to V_{CC}
I_{OZL}	3-STATE Output Leakage Current	3.6		−5	μA	V_O = 0.5V
I_{OZL} (Note 5)	3-STATE Output Leakage Current	3.6		−5	μA	V_O = 0.0V
I_{OZH}	3-STATE Output Leakage Current	3.6		5	μA	V_O = 3.0V
I_{OZH} (Note 5)	3-STATE Output Leakage Current	3.6		5	μA	V_O = 3.6V
I_{OZH}+	3-STATE Output Leakage Current	3.6		10	μA	$V_{CC} < V_O \le 5.5V$
I_{CCH}	Power Supply Current	3.6		0.19	mA	Outputs HIGH
I_{CCL}	Power Supply Current	3.6		5	mA	Outputs LOW
I_{CCZ}	Power Supply Current	3.6		0.19	mA	Outputs Disabled
I_{CCZ}+	Power Supply Current	3.6		0.19	mA	$V_{CC} < V_O \le 5.5V$, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 8)	3.6		0.2	mA	One input at V_{CC} − 0.6V Other inputs at V_{CC} or GND

Note 5: Applies to Bushold versions only (74LVTH162245).
Note 6: An external driver must source at least the specified current to switch from LOW-to-HIGH.
Note 7: An external driver must sink at least the specified current to switch from HIGH-to-LOW.
Note 8: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 9)

Symbol	Parameter	V_CC (V)	T_A = 25°C			Units	Conditions C_L = 50 pF, R_L = 500Ω
			Min	Typ	Max		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 10)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 10)

Note 9: Characterized in SSOP package. Guaranteed parameter, but not tested.
Note 10: Max number of outputs defined as (n). n−1 data inputs are driven 0V to 3V. Output under test held LOW.

The left margin has vertical text: 74LVT162245 • 74LVTH162245

74LVT162245 • 74LVTH162245

AC Electrical Characteristics

$T_A = -40°C$ to $+85°C$

$C_L = 50$ pF, $R_L = 500\Omega$

| Symbol	Parameter	$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		Units
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Data to A Port Output	1.0	4.0	1.0	4.6	ns
t_{PHL}		1.0	3.7	1.0	4.1	
t_{PLH}	Propagation Delay Data to B Port Output	1.0	3.5	1.0	3.9	ns
t_{PHL}		1.0	3.5	1.0	3.9	
t_{PZH}	Output Enable Time for A Port Output	1.0	5.3	1.0	6.3	ns
t_{PZL}		1.0	5.6	1.0	7.2	
t_{PZH}	Output Enable Time for B Port Output	1.0	4.6	1.0	5.4	ns
t_{PZL}		1.0	5.3	1.0	6.9	
t_{PHZ}	Output Disable Time for A Port Output	1.5	5.6	1.5	6.3	ns
t_{PLZ}		1.5	5.5	1.5	5.5	
t_{PHZ}	Output Disable Time for B Port Output	1.5	5.4	1.5	6.1	ns
t_{PLZ}		1.5	5.1	1.5	5.4	
t_{OSHL}	A Port Output to Output Skew		1.3.7	1.01.0		

Note 11: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Capacitance   (Note 12)

Note 12: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

Physical Dimensions   inches (millimeters) unless otherwise noted

Top
View

PIN ONE

Bottom
View

54X 0.5$^{+0.05}_{-0.05}$

SEATING PLANE

1.4MAX

0.45
0.35
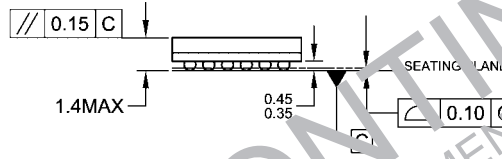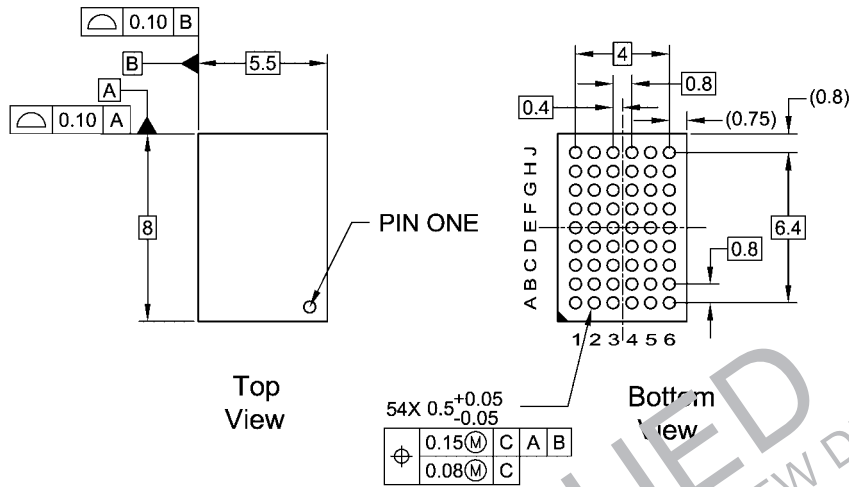
NOTES:
A. THIS PACKAGE CONFORMS TO JEDEC MO-205

54-Ball Fine Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
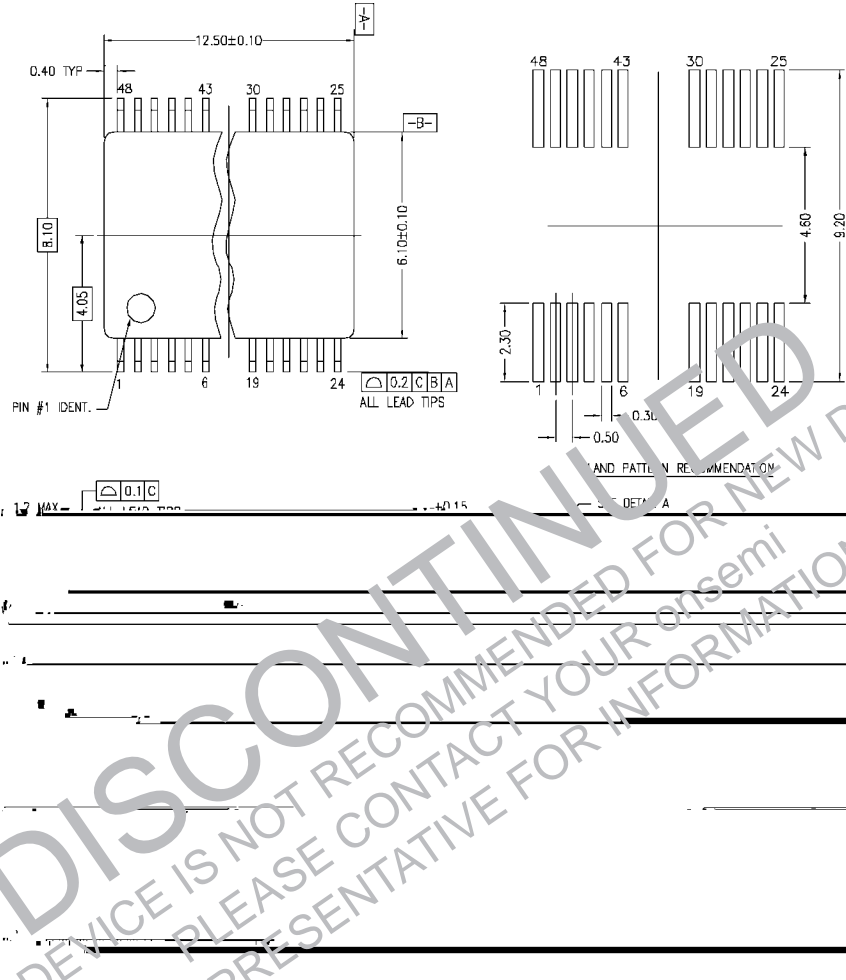Package Number BGA54A

Physical Dimensions

Physical Dimensions   inches (millimeters) unless otherwise noted (Continued)

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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