June 2005
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74LCXP16245
Low Voltage 16-Bit Bidirectional Transceiver with 5V Tolerant Inputs/Outputs and Pull-Down Resistors

General Description

The LCXP16245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The device is byte controlled. Each byte has separate control inputs which could be shorted together for full 16-bit operation. The T/$\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

In addition, A and B port datapath pins have built-in resistors to GND allowing the pins to float without any increase in I_{CC} current. This feature is intended to address modular and space constrained applications where additional space consumed by external resistors is not available.

The LCXP16245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

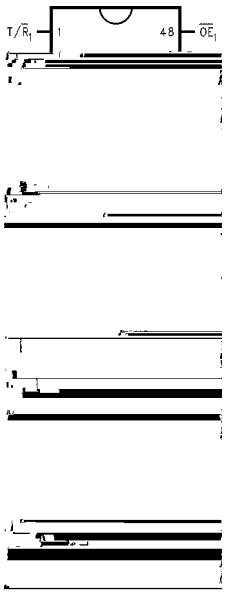
- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- I/O pull-down resistors terminate inactive busses ensuring a stable bus state
- 5.5 ns t_{PD} max (V_{CC} = 3.3V), 20 μA I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ±24 mA output drive (V_{CC} = 3.0V)
- Pinout compatible with 74 series 16245
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

Note 1: To ensure the high-impedance state during power up or down $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the orino co00Viix00Vode945 36.4 1 T (l(ix)-11.or t)Descr (he)]T120.0219 Tc 5.0017 Tw 6.96 0 0 1 0 4102489 5.2901 Tm (l)-

Connection Diagram



Truth Tables

Inputs $\overline{OE}_1$	Inputs $T/\overline{R}_1$	Outputs
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7 (Note 2)

651.49 i-13A.96 0 0 6.96 392.97 553.29 Tm c5.25 565.77 Tm (2)T

Inputs $\overline{OE}_2$	Inputs $T/\overline{R}_2$	Outputs
L	L	Bus B_8–B_{15} Data to Bus A_8

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Note 2: A and B port inputs are still active.

Functional Descriptions

The LCXP16245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs. the device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The T/$\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state. The pulldown resistor (30KΩ normal) to GND is active only when the outputs are 3-STATED ($\overline{OE}$ = HIGH). When the outputs become active ($\overline{OE}$ = LOW) the resistor is removed from the circuit.

Logic Diagram

Absolute Maximum Ratings(Note 3)

Recommended Operating Conditions

Note 3:

DC Electrical Characteristics (Continued)

Note 5: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Note 6:

AC LOADING and WAVEFORMS Generic for LCX Family

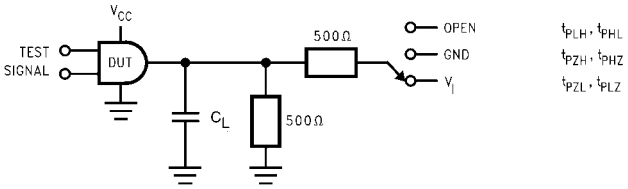
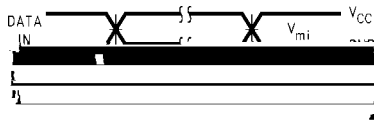
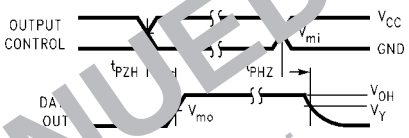


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

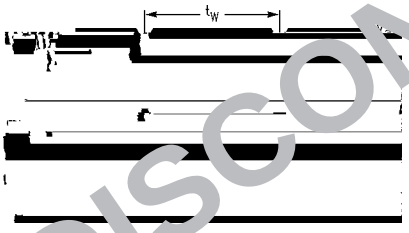
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V
t_{PZH}, t_{PHZ}	GND



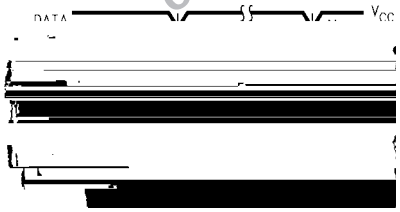
Waveform for Inverting and Non-Inverting Functions



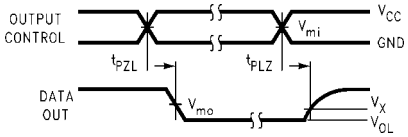
3-STATE Output High Enable and Disable Times for Logic



Propagation Delay, Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



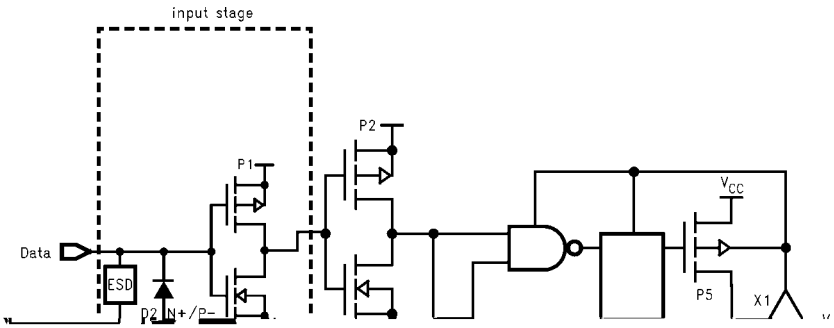
3-STATE Output Low Enable and Disable Times for Logic

t_{rise} and t_{fall}

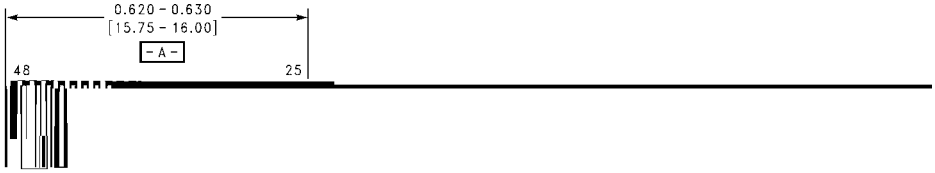
FIGURE 2. Waveforms
(Input Characteristics; f = 1MHz, t_r = t_f = 3ns)

Symbol	V_{CC}		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V_{mi}	1.5V	1.5V	V_{CC}/2
V_{mo}	1.5V	1.5V	V_{CC}/2
V_x	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V
V_y	V_{OH} − 0.3V	V_{OH} − 0.3V	V_{OH} − 0.15V

Schematic Diagram Generic for LCX Family

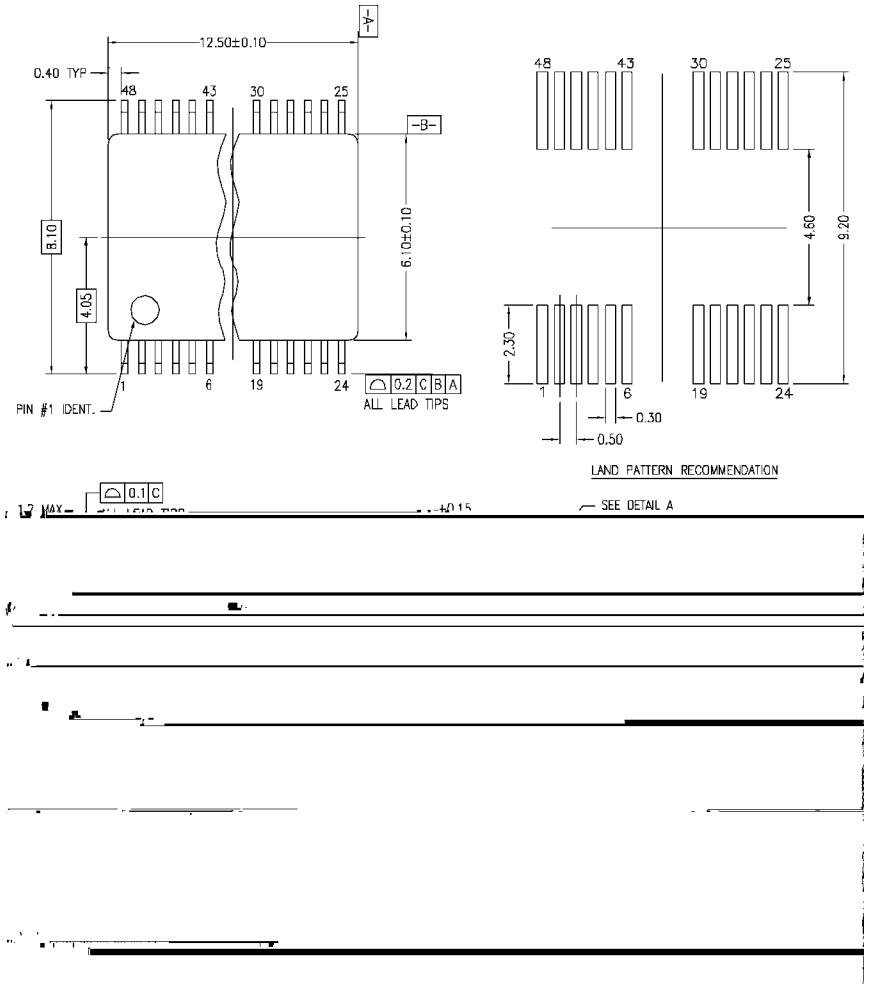


Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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