March 2001
Revised August 2024

74LCX821
Low Voltage 10-Bit D-Type Flip-Flop with 5V Tolerant Inputs and Outputs

General Description

The LCX821 consists of ten D-type Flip-Flops with 3-STATE outputs for bus organized system applications. The device is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX821 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 7.0 ns t_{PD} max (V_{CC} = 3.3V), 10 µA I_{CC} max
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ±24 mA output drive (V_{CC} = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human Body Model > 2000V
  - Machine Model > 200V

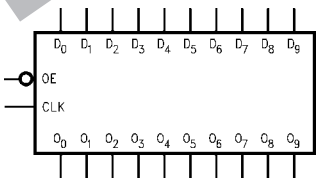
Note 1: To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

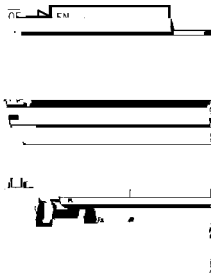
Order Number	Package Number	Package Description
74LCX821WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74LCX821MSA	MSA24	24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LCX821MTC	MTC2	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix "X" to the ordering code.

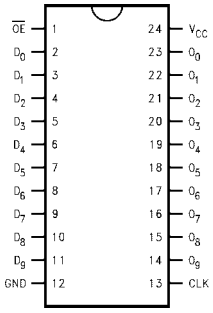
Logic Symbols



IEEE/IEC



Connection Diagram



Pin Descriptions

Pin Names	Description
D_0–D_9	Data Inputs
CLK	Clock Input
$\overline{OE}$	Output Enable Input
O_0–O_9	3-STATE Latch Outputs

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CLK	D	Q	O_n	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↗	L	L	9.29 44c5.6 3801y 186901 63.57 0.48 [illegible]	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impendance
↗ = LOW-to-HIGH Transition
NC = No Change

Functional Description

The LCX821 consists of ten edge-triggered flip-flops with individual D-type inputs with 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The ten flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CLK) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the ten flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Logic Diagram

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to V_{CC} + 0.5	Output in HIGH or LOW State (Note 3)	
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA

Recommended Operating Conditions (Note 4)

Note 2: The Absolute Maximum Ratings are the values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$ Min	Max	Units
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 3.6		10	µA
		$3.6V \le V_I$, $V_O \le 5.5V$ (Note 5)	2.3 – 3.6		±10	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.3 – 3.6		500	µA

Note 5: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$ $V_{CC} = 3.3V \pm 0.3V$, $C_L = 50$ pF Min	Max	$V_{CC} = 2.7V$, $C_L = 50$ pF Min	Max	$V_{CC} = 2.5V \pm 0.2V$, $C_L = 30$ pF Min	Max	Units
f_{MAX}	Maximum Clock Frequency	150						MHz
t_{PHL}	Propagation Delay	1.5	7.0	1.5	7.5	1.5	8.4	ns
t_{PLH}	CLK to O_n	1.5	7.0	1.5	7.5	1.5	8.4	
t_{PZL}	Output Enable Time	1.5	7.5	1.5	8.0	1.5	9.8	ns
t_{PZH}		1.5	7.5	1.5	8.0	1.5	9.8	
t_{PLZ}	Output Disable Time	1.5	6.5	1.5	7.0	1.5	7.8	ns
t_{PHZ}		1.5	6.5	1.5	7.0	1.5	7.8	
t_{OSHL}	Output to Output Skew		1.0					ns
t_{OSLH}	(Note 6)		1.0					
t_S	Setup Time, D_n to CLK	2.5		2.5		4.0		ns
t_H	Hold Time, D_n to CLK	1.5		1.5		2.0		ns
t_W	CLK Pulse Width	3.3		3.3		4.0		ns

Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, V_{IH} = 32p9 0 Tm [(OL)-22 (]TJ 0 Tp<37 0.9yu3 Tc 0 Tw 4.7995 0 0 4.7995 316.41 337.89 41.)IH 32p9 0 Tm [(O0			

Capacitance

AC LOADING and WAVEFORMS Generic for LCX Family

FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

Waveform for Inverting and Non-Inverting Functions

3-STATE Output High Enable and Disable Times for Logic

Propagation Delay. Pulse Width and t_{rec} Waveforms

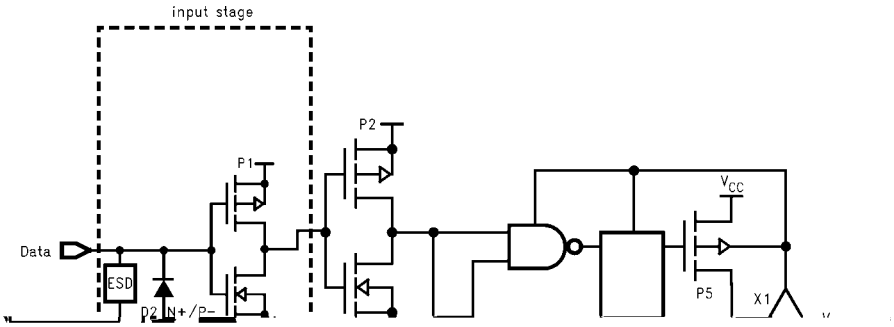
Setup Time, Hold Time and Recovery Time for Logic

3-STATE Output Low Enable and Disable Times for Logic

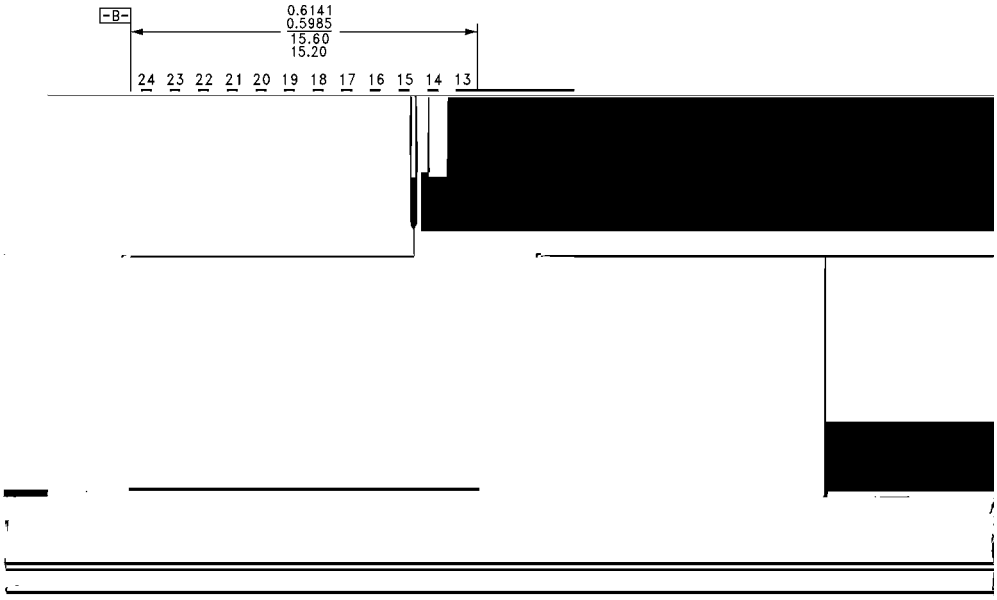
t_{rise} and t_{fall}

Ds f1 1 Tf sab13.1 0 witc

Schematic Diagram Generic for LCX Family



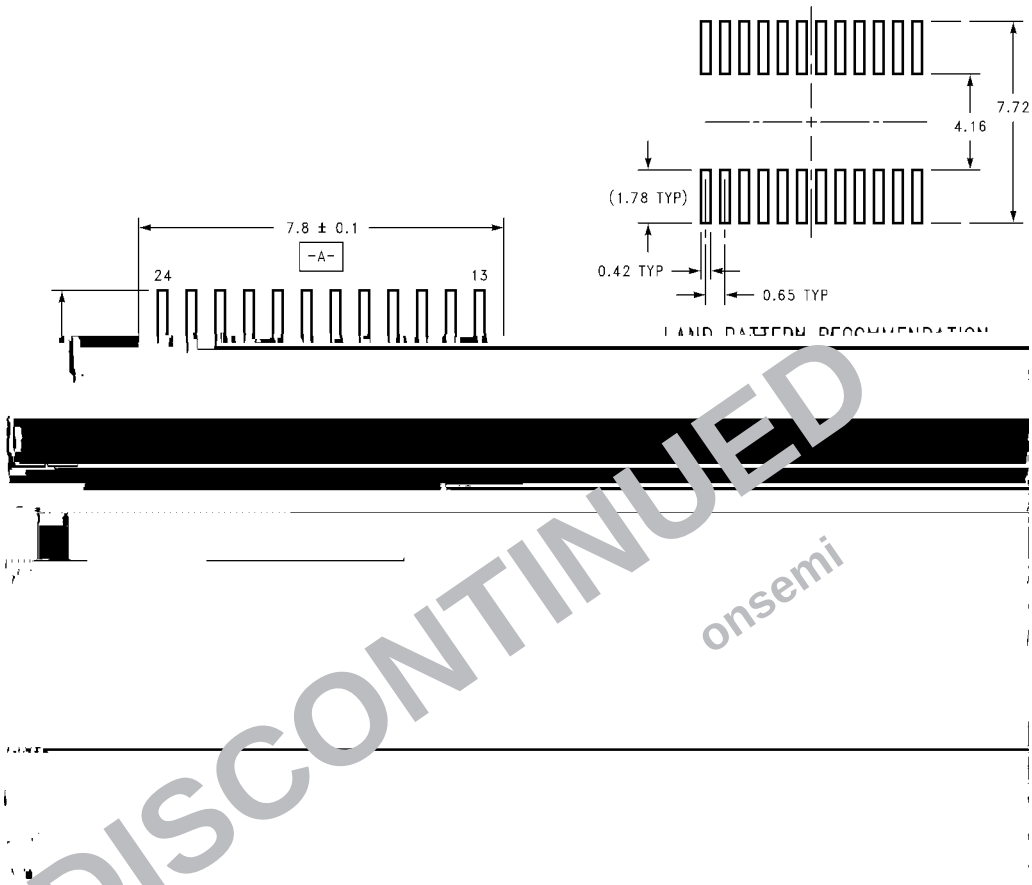
Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B

24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA24

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24