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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

## Features

- 5V tolerant inputs and outputs
- 2.3V – 3.6V $V_{CC}$ specifications provided
- 7.0 ns $t_{PD}$ max ($V_{CC}$ = 3.3V), 10 µA $I_{CC}$ max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ±24 mA Output Drive ($V_{CC}$ = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

**Note 1:** To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to $V_{CC}$ through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

## Ordering Code:

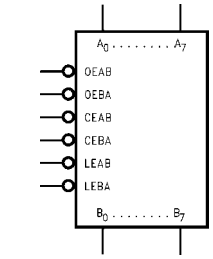
| Order Number | Package Number | Package Description |
|---|---|---|
| 74LCX543WM | M24B | 24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| 74LCX543MSA | MSA24 | 24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide |

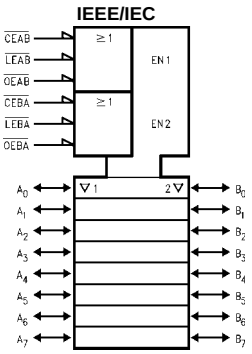
Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

## Connection Diagram

## Pin Descriptions

## Logic Symbols




## Data I/O Control Table

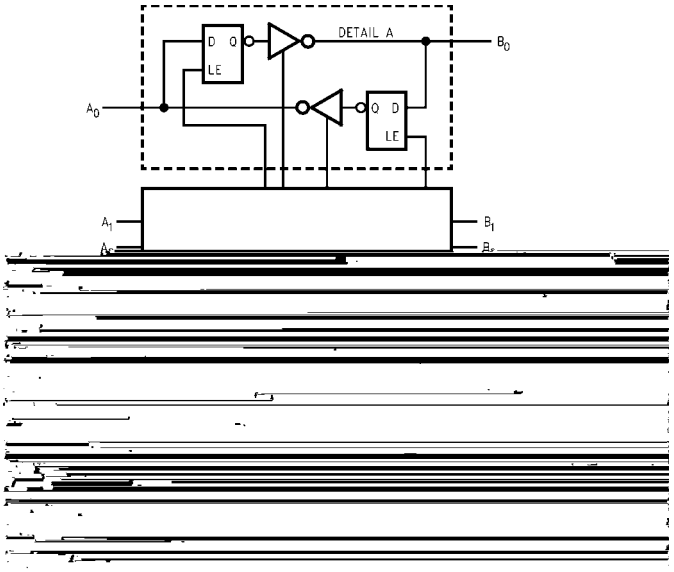
| Inputs | | | Latch Status | Output Buffers |
|---|---|---|---|---|
| $\overline{CEAB}$ | $\overline{LEAB}$ | $\overline{OEAB}$ | | |
| H | X | X | Latched | High Z |
| X | H | X | Latched | — |
| L | L | X | Transparent | — |
| X | X | H | — | High Z |
| L | X | L | — | Driving |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$

## Functional Description

The LCX543 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from $A_0$–$A_7$ or take data from $B_0$–$B_7$, as indicated in the Data I/O Control Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

## Logic Diagram




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## DC Electrical Characteristics (Continued)

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A = -40°C$ to $+85°C$ Min | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent Supply Current | $V_I = V_{CC}$ or GND | 2.3 – 3.6 | | 10 | µA |
| | | $3.6V \le V_I, V_O \le 5.5V$ (Note 5) | 2.3 – 3.6 | | ±10 | |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | $V_{IH} = V_{CC} - 0.6V$ | 2.3 – 3.6 | | 500 | µA |

**Note 5:** Outputs disabled or 3-STATE only.

## AC Electrical Characteristics

| Symbol | Parameter | $T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$ $V_{CC} = 3.3V \pm 0.3V$ $C_L = 50$ pF Min | Max | $V_{CC} = 2.7V$ $C_L = 50$ pF Min | Max | $V_{CC} = 2.5V \pm 0.2V$ $C_L = 30$ pF Min | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation Delay | 1.5 | 7.0 | 1.5 | 8.0 | 1.5 | 8.4 | ns |
| $t_{PLH}$ | $A_n$ to $B_n$ or $B_n$ to $A_n$ | 1.5 | 7.0 | 1.5 | 8.0 | 1.5 | 8.4 | |
| $t_{PHL}$ | Propagation Delay | 1.5 | 8.5 | 1.5 | 9.5 | 1.5 | 10.5 | ns |
| $t_{PLH}$ | $\overline{LEBA}$ to $A_n$ or $\overline{LEAB}$ to $B_n$ | 1.5 | 8.5 | 1.5 | 9.5 | 1.5 | 10.5 | |
| $t_{PZL}$ | Output Enable Time | 1.5 | 9.0 | 1.5 | 10.0 | 1.5 | 11.0 | ns |
| $t_{PZH}$ | $\overline{OEBA}$ or $\overline{OEAB}$ to $A_n$ or $B_n$ | 1.5 | 9.0 | 1.5 | 10.0 | 1.5 | 11.0 | |
| | $\overline{CEBA}$ or $\overline{CEAB}$ to $A_n$ or $B_n$ | | | | | | | |
| $t_{PLZ}$ | Output Disable Time | 1.5 | 7.0 | 1.5 | 7.5 | 1.5 | 8.4 | ns |
| $t_{PHZ}$ | $\overline{OEBA}$ or $\overline{OEAB}$ to $A_n$ or $B_n$ | 1.5 | 7.0 | 1.5 | 7.5 | 1.5 | 8.4 | |
| | $\overline{CEBA}$ or $\overline{CEAB}$ to $A_n$ or $B_n$ | | | | | | | |
| $t_S$ | Setup Time, HIGH or LOW Data to $\overline{LEXX}$ | 2.5 | | 2.5 | | 4.0 | | ns |
| $t_H$ | Hold Time, HIGH or LOW Data to $\overline{LEXX}$ | 1.5 | | 1.5 | | 2.0 | | ns |
| $t_W$ | Pulse Width, Latch Enable, LOW | 3.3 | | 3.3 | | 3.3 | | ns |
| $t_{OSHL}$ | Output to Output Skew | | 1.0 | | | | | ns |
| $t_{OSLH}$ | (Note 6) | | 1.0 | | | | | |

**Note 6:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ($t_{OSHL}$) or LOW-to-HIGH ($t_{OSLH}$).

## Dynamic Switching Characteristics

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A = 25°C$ Typical | Units |
|---|---|---|---|---|---|
| $V_{OLP}$ | Quiet Output Dynamic Peak $V_{OL}$ | $C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$ | 3.3 | 0.8 | V |

C

m 0 Tc9(i60D (C/ T)s701 Tm 0 Tc9(i60 5l19 303.8101 Tm -0.0029 Tc 0 Tw (OL)Tj 6 8f6 Tfkj -34.76 .894.9(ic P)-11.1(e)17.9(D ( )Tput)380D (C/ 0)-1.2(.8E9B4mcC)11.1(on)2t9oZ7 326.4901 Tm ( )Tj /F5 1t)3o5L2S71 Tc9(801 3)-11.1
4a3j 4.77C

## Capacitance

## AC LOADING and WAVEFORMS Generic for LCX Family

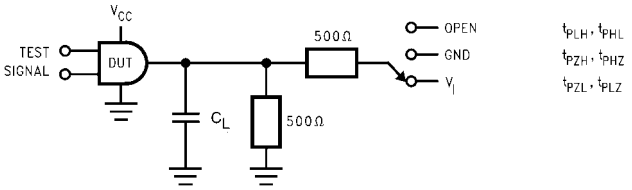
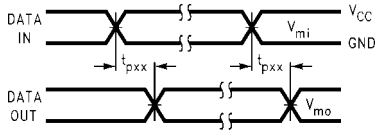
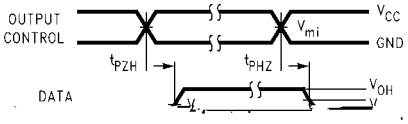



**FIGURE 1. AC Test Circuit ($C_L$ includes probe and jig capacitance)**

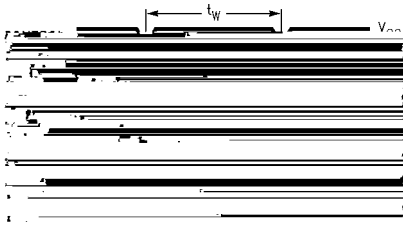
| Test | Switch |
|---|---|
| $t_{PLH}$, $t_{PHL}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | 6V at $V_{CC}$ = 3.3 ± 0.3V<br>$V_{CC}$ x 2 at $V_{CC}$ = 2.5 ± 0.2V |
| $t_{PZH}$,$t_{PHZ}$ | GND |



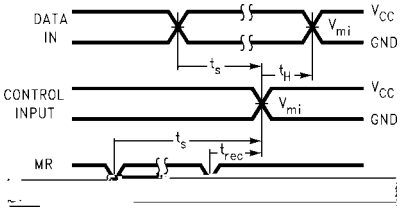

**Waveform for Inverting and Non-Inverting Functions**



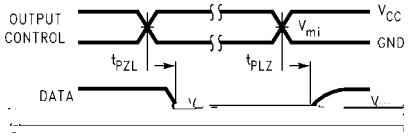

**3-STATE Output High Enable and Disable Times for Logic**



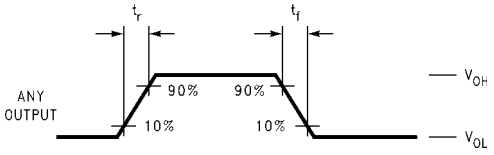

**Propagation Delay. Pulse Width and $t_{rec}$ Waveforms**




**Setup Time, Hold Time and Recovery Time for Logic**




**3-STATE Output Low Enable and Disable Times for Logic**



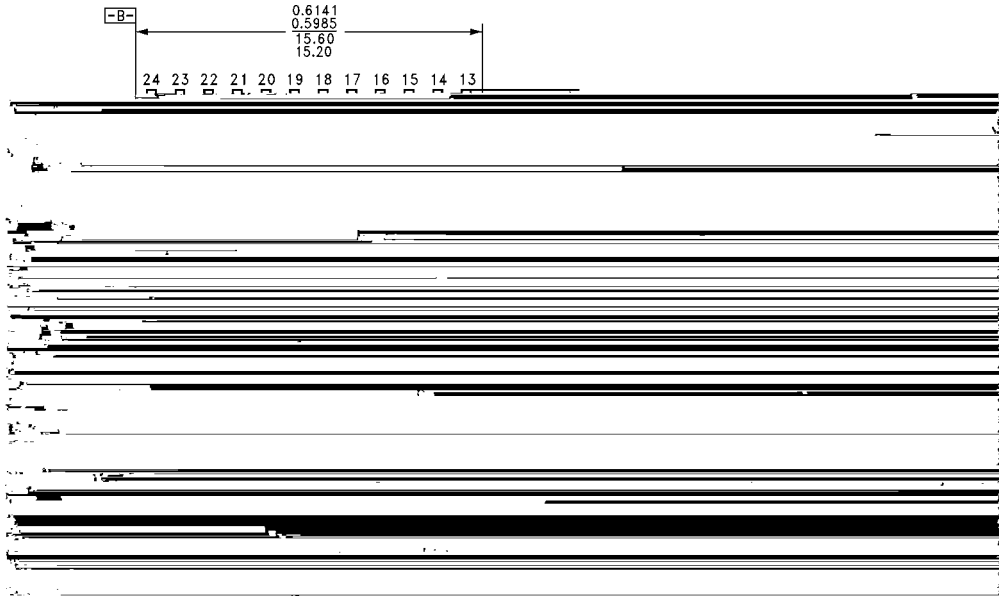

**$t_{rise}$ and $t_{fall}$**

**FIGURE 2. Waveforms**
**(Input Characteristics; f =1MHz, $t_R$ = $t_F$ = 3ns)**

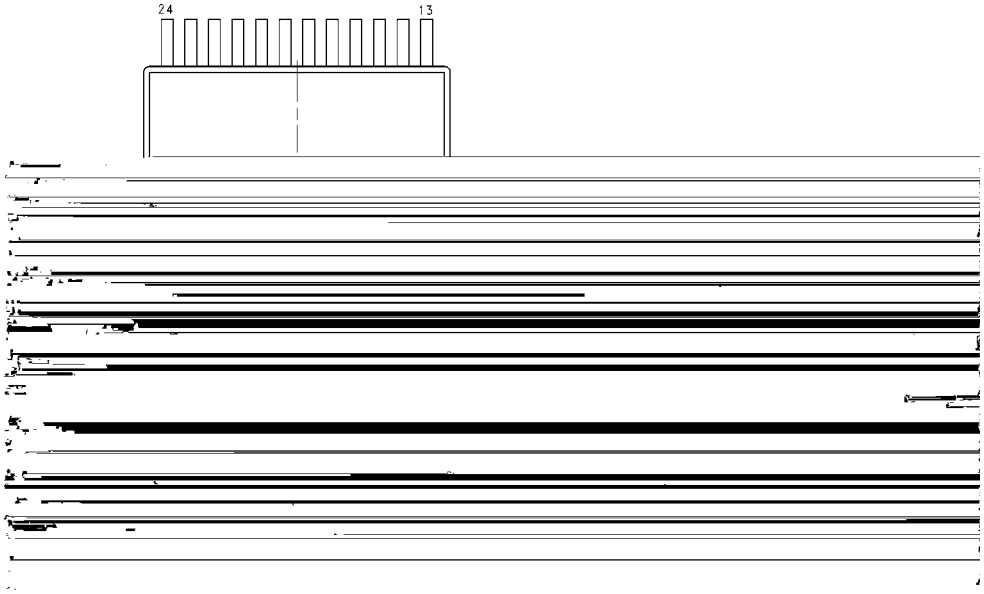
| Symbol | $V_{CC}$ | | |
|---|---|---|---|
| | **3.3V ± 0.3V** | **2.7V** | **2.5V ± 0.2V** |
| $V_{mi}$ | 1.5V | 1.5V | $V_{CC}$/2 |
| $V_{mo}$ | 1.5V | 1.5V | $V_{CC}$/2 |
| $V_x$ | $V_{OL}$ + 0.3V | $V_{OL}$ + 0.3V | $V_{OL}$ + 0.15V |
| $V_y$ | $V_{OH}$ − 0.3V | $V_{OH}$ − 0.3V | $V_{OH}$ − 0.15V |

## Schematic Diagram Generic for LCX Family

## Physical Dimensions inches (millimeters) unless otherwise noted




**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide**
**Package Number M24B**




**24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number MSA24**

## Physical Dimensions

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