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Low Voltage Hex Buffer with Open Drain Outputs

74LCX07

General Description

The LCX07 contains six buffers. The inputs tolerate voltages up to 5.5 V allowing the interface of 5 V systems to 3 V systems.

The outputs of the LCX07 are open drain and can be connected to other open drain outputsto implement active HIGH wire AND or active LOW wire OR functions.

The 74LCX07 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5 V Tolerant Inputs
- 1.65 V – 5.5 V V_{CC} Specifications Provided
- 2.9 ns t_{PD} Max. (V_{CC} = 3.3 V), 10 μA I_{CC} Max.
- Power Down High Impedance Inputs and Outputs
- ±24 mA Output Drive (V_{CC} = 3.0 V)
- Implements Proprietary Noise/EMI Reduction Circuitry
- Latch−up Performance Exceeds JEDEC 78 Conditions
- ESD performance:
  - Human Body Model >2000 V

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CONNECTION DIAGRAMS

Figure 1. Pin Assignments for SOIC and TSSOP

(Top View) (Bottom View)

Figure 2. Pad Assignments for DQFN

ABSOLUTE MAXIMUM RATINGS

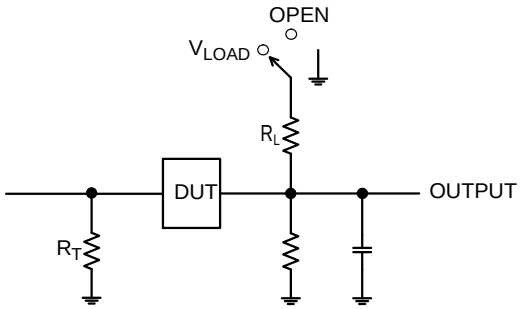
Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_I	DC Input Voltage (Note 1)		−0.5 to +6.5	V
V_O	DC Output Voltage (Note 1)	Active−Mode (High or Low State) Tri−State Mode Power−Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} + 0.5 −0.5 to +6.5 −0.5 to +6.5	V
I_{IK}	DC Input Diode Current	V_I < GND	−50	mA
I_{OK}	DC Output Diode Current	V_O < GND	−50	
I_O	DC Output Source/Sink Current		±50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin			

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		T_A = −40°C to +125°C		Unit
				Min	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage		1.65 – 1.95	0.65 x V_{CC}	−	0.65 x V_{CC}	−	V
			2.3 – 2.7	1.7	−	1.7	−	
			3.0 – 3.6	2.0	−	2.0	−	
			4.5 − 5.5	0.70 x V_{CC}	−	0.70 x V_{CC}	−	
V_{IL}	LOW Level Input Voltage		1.65 – 1.95	−	0.35 x V_{CC}	−	0.35 x V_{CC}	V
			2.3 – 2.7	−	0.7	−	0.7	
			3.0 – 3.6	−	0.8	−	0.8	
			4.5 − 5.5	−	0.30 x V_{CC}	−	0.30 x V_{CC}	
V_{OL}	Low−Level Output Voltage	V_I = V_{IH} or V_{IL}						V
		I_{OL} = 100 μA	1.65 − 5.5	−	0.1	−	0.1	
		I_{OL} = 4 mA	1.65	−	0.24	−	0.24	
		I_{OL} = 8 mA	2.3	−	0.3	−	0.3	
		I_{OL} = 12 mA	2.7	−	0.4	−	0.4	
		I_{OL} = 16 mA	3.0	−	0.4	−	0.4	
		I_{OL} = 24 mA	3.0	−	0.55	−	0.55	
		I_{OL} = 32 mA	4.5	−	0.6	−	0.6	
I_I	Input Leakage Current	V_I = 0 to 5.5 V	1.65 − 5.5	−	±5.0	−	±5.0	μA
I_{OZ}	Off−State Leakage Current	V_O = 5.5 V	1.65 − 5.5	−	10	−	10	μA
I_{OFF}	Power Off Leakage Current	V_I = 5.5 V or V_O = 5.5 V	0	−	10	−	10	μA
I_{CC}	Quiescent Supply Current	V_I = 5.5 V or GND	5.5	−	10	−	10	

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V


OPEN
V_{LOAD}
R_L
DUT
OUTPUT
R_T

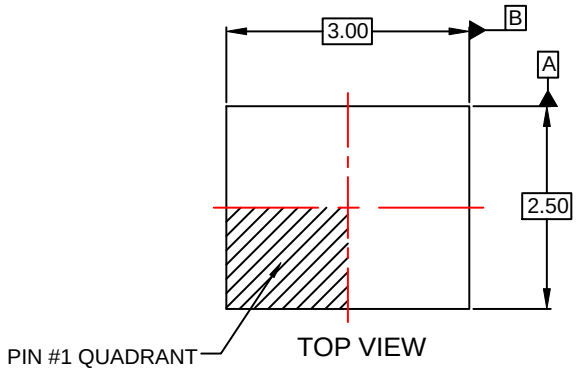
ORDERING INFORMATION

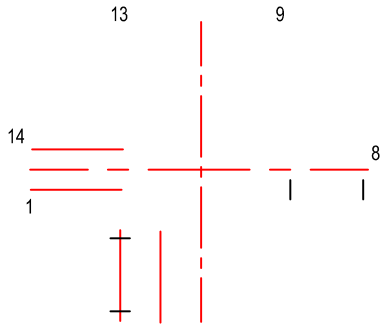
Device	Marking	Package	Shipping†
74LCX07MTCX	LCX 07	TSSOP−14	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

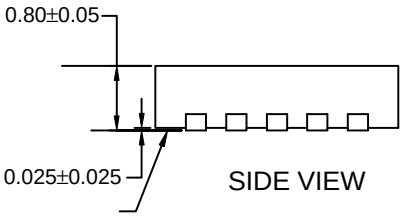
QFN14 3.0x2.5, 0.5P
CASE 510CB
ISSUE O

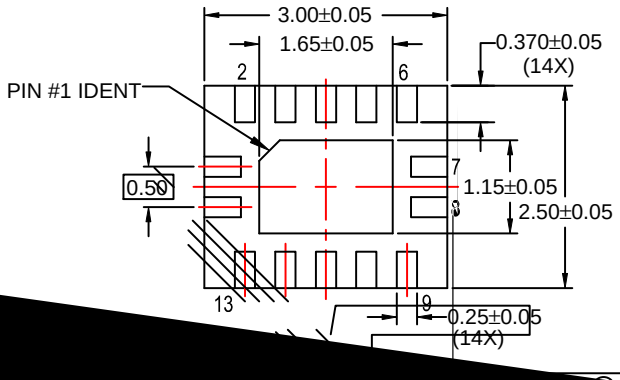
DATE 31 AUG 2016





RECOMMENDED LAND PATTERN





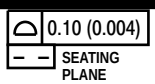
NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−241, VARIATION AA

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.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0.10 (0.004)
SEATING
PLANE

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