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74AUP1G57 TinyLogic[®] Low Power Universal Configurable Two-Input Logic Gate

Features

- Š 0.8V to 3.6V V_{CC} Supply Operation
- \check{S} $\,$ 3.6V Over-Voltage Tolerant I/Os at V_CC from 0.8V to 3.6V
- Š High Speed tpd
 - 2.9ns: Typical at 3.3V
- Š Power-Off High-Impedance Inputs and Outputs
- Š Low Static Power Consumption
 - I_{CC}=0.9µA Maximum
- Š Low Dynamic Power Consumption
 - C_{PD}=2.9pF Typical at 3.3V
- Š Ultra-Small MicroPak™ Packages

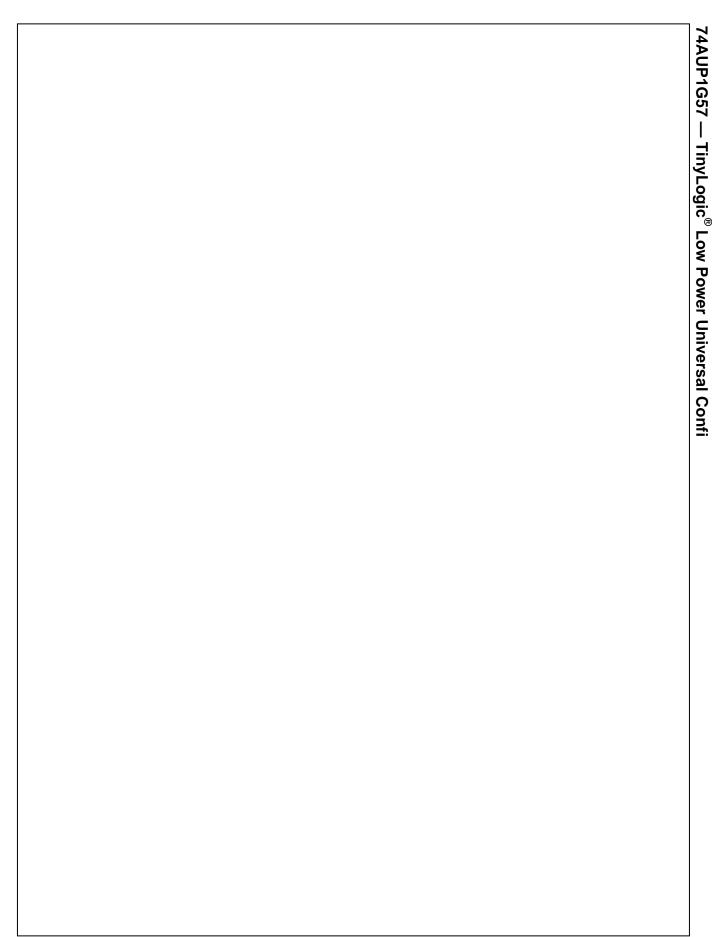
Description

The 74AUP1G57 is a universal configurable 2-input logic gate that provides a high performance and low power solution ideal for battery-powered portable applications. This product is designed for a wide low voltage operating range (0.8V to 3.6V) and guarantees very low static and dynamic power consumption across the entire voltage range. All inputs are implemented with hysteresis to allow for slower transition input signals and better switching noise immunity.

The 74AUP1G57 provides for multiple functions as determined by various configurations of the three inputs. The potential logic functions provided are AND, NAND, OR, NOR, and XNOR, inverter and buffer. Refer to Figures 2 to 8.

Ordering Information

| Part Number | Top Mark | Package | Packing Method |
|--------------|----------|---|------------------------------|
| 74AUP1G57L6X | AB | 6-Lead Micropak™, 1.0mm Wide | 5000 Units on Tape & Reel |
| 74AUP1G57FHX | AB | 6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch | 5000 Units on Tape & Reel |



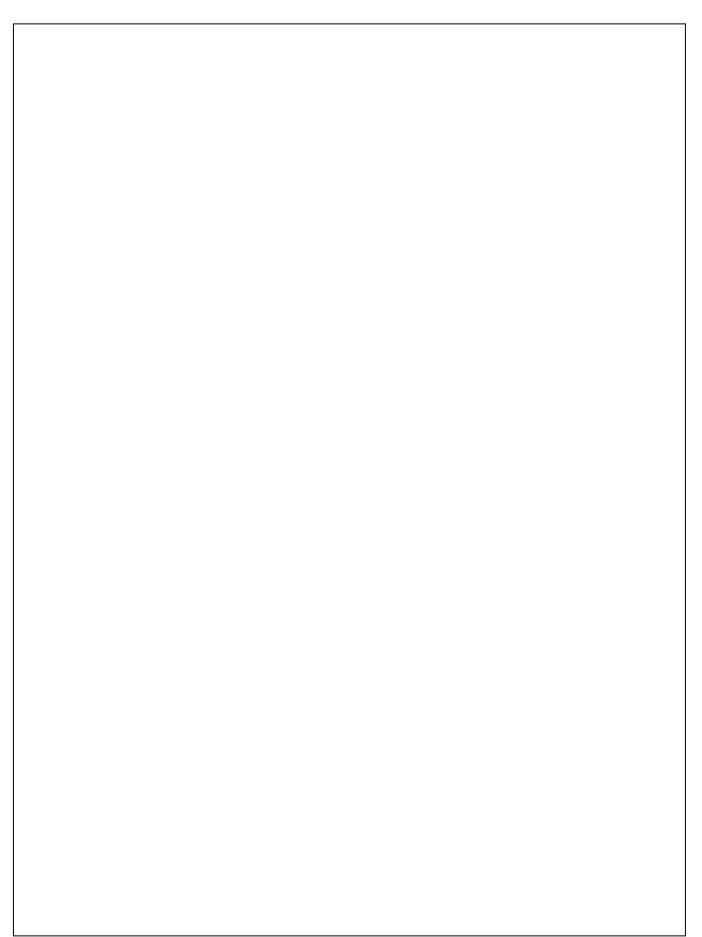
Function Table

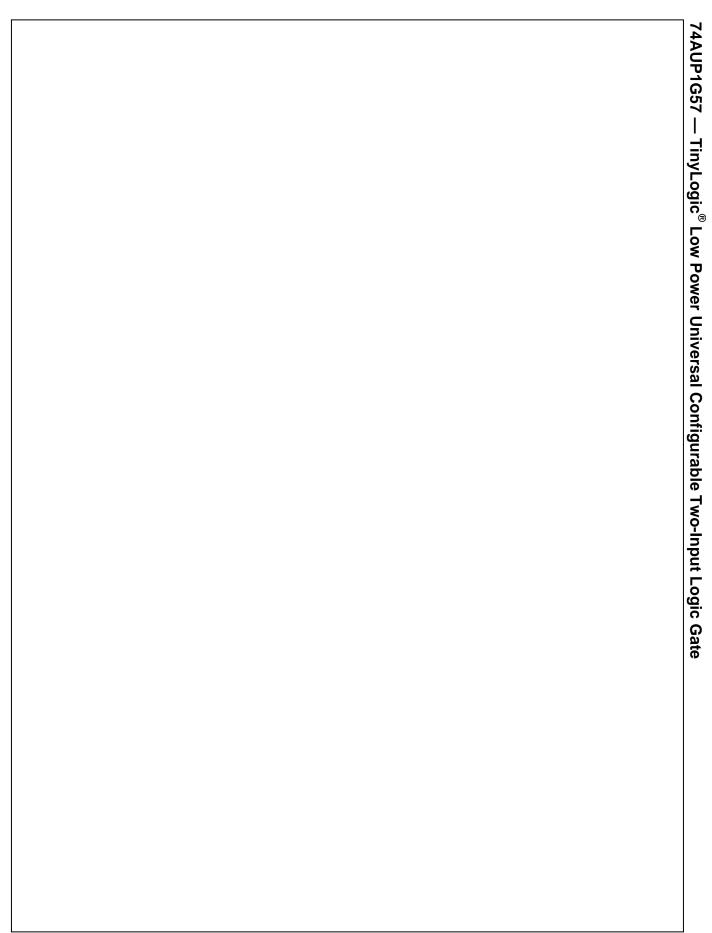
| Inputs | | | 74AUP1G57 | |
|--------|---|---|-----------|--|
| С | В | Α | Y=Output | |
| L | L | L | Н | |
| L | L | Н | L | |
| L | Н | L | Н | |
| L | Н | Н | L | |
| Н | L | L | L | |
| Н | L | Н | L | |
| Н | Н | L | Н | |
| Н | Н | Н | Н | |

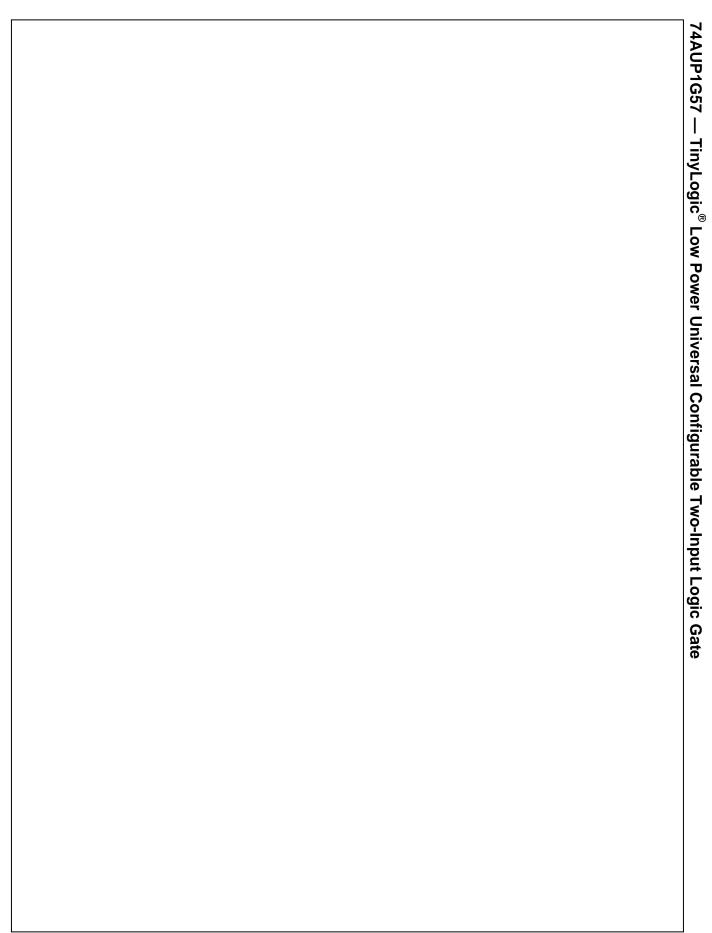
H = HIGH Logic Level L = LOW Logic Level

Function Selection Table

| 2-Input Logic Function | Connection Configuration | |
|---------------------------------------|--------------------------|--|
| 2-Input AND | Figure 2 | |
| 2-Input AND with Both Inputs Inverted | Figure 5 | |
| 2-Input NAND with Inverted Input | Figure 3, Figure 4 | |
| 2-Input OR with Inverted Input | Figure 3, Figure 4 | |
| 2-Input NOR | Figure 5 | |
| 2-Input NOR with Both Inputs Inverted | Figure 2 | |
| 2-Input XNOR | Figure 6 | |
| Inverter | Figure 7 | |
| Buffer | Figure 8 | |

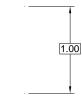






| AC Loadings and Waveforms | 1 |
|---------------------------|------------------|
| | |
| | Illycogic |
| | יר ביאר ביירי |
| | CWG |
| | CHIVELSAI |
| | |
| | Comiguiable |
| | - w C- |
| | - wo-inpar Logic |
| | טמופ |
| | |
| | |
| | |
| | |

Physical Dimensions



- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

