

74AC04, 74ACT04

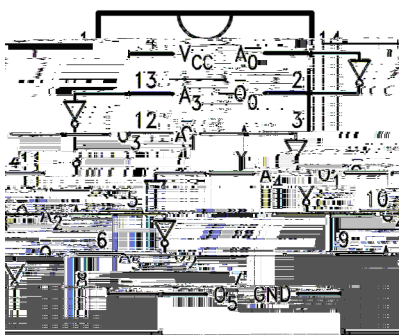


Figure 1. Connection Diagram

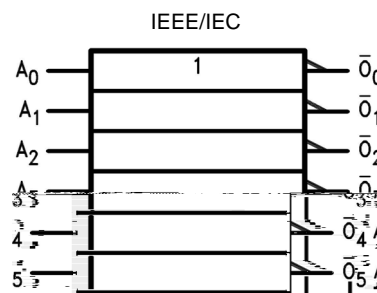


Figure 2. Logic Symbol

PIN DESCRIPTION

Pin	Description
A_n	Inputs
\bar{O}_n	Outputs

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage AC ACT	2.0 4.5	6.0 5.5	V
V_I	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	-40	+85	°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices: V_{IN} from 30% to 70% of V_{CC} , V_{CC} at 3.3 V, 4.5 V, 5.5 V	125		mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices: V_{IN} from 0.8 V to 2.0 V, V_{CC} at 4.5 V, 5.5 V	125		mV/ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond

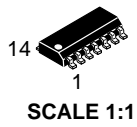
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DC ELECTRICAL CHARACTERISTICS FOR ACT

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C		T _A = -40°C to +85°C		Unit
				Typ	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage	4.5	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	1.5	2.0	2.0		V
		5.5		1.5	2.0	2.0		
V _{IL}	Maximum LOW Level Input Voltage	4.5	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	1.5	0.8	0.8		V
		5.5		1.5	0.8	0.8		
V _{OH}	Minimum HIGH Level Output Voltage	4.5	I _{OUT} = -50 μA	4.49	4.4	4.4		V
		5.5		5.49	5.4	5.4		
		4.5	V _{IN} = V _{IL} or V _{IH} I _{OH} = -24 mA	-	3.86	3.76		
		5.5	I _{OH} = -24 mA (Note 4)	-	4.86	4.76		
V _{OL}	Maximum LOW Level Output Voltage	4.5	I _{OUT} = 50 μA	0.001	0.1	0.1		V
		5.5		0.001	0.1	0.1		
		4.5	V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA	-	0.36	0.44		
		5.5	I _{OL} = 24 mA (Note 4)	-	0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5	V _I = V _{CC} , GND	-	±0.1	±1.0		μA
I _{CCT}	Maximum I _{CC} /Input	5.5	V _I = V _{CC} - 2.1 V	0.6	-	1.5		mA
I _{OLD}	Minimum Dynamic Output Current (Note 5)	5.5	V _{OLD} = 1.65 V Max.	-	-	75		mA
I _{OHD}		5.5	V _{OHD} = 3.85 V Min.	-	-	-75		mA
I _{CC}	Maximum Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND	-	4.0	40.0		μA

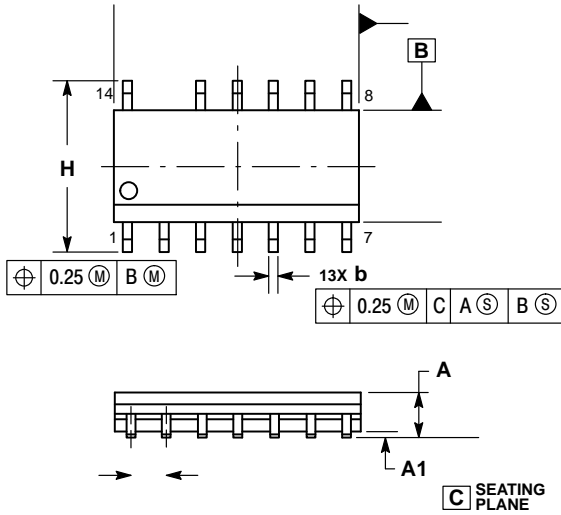
4. All outputs loaded; thresholds on input associated with output under test.

5. Maximum test duration 2.0 ms, one output loaded at a time.



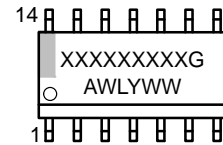
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CASE 751A-03
ISSUE L

DATE 03 FEB 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

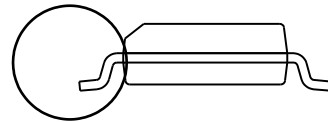
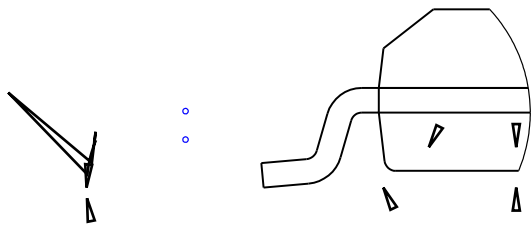
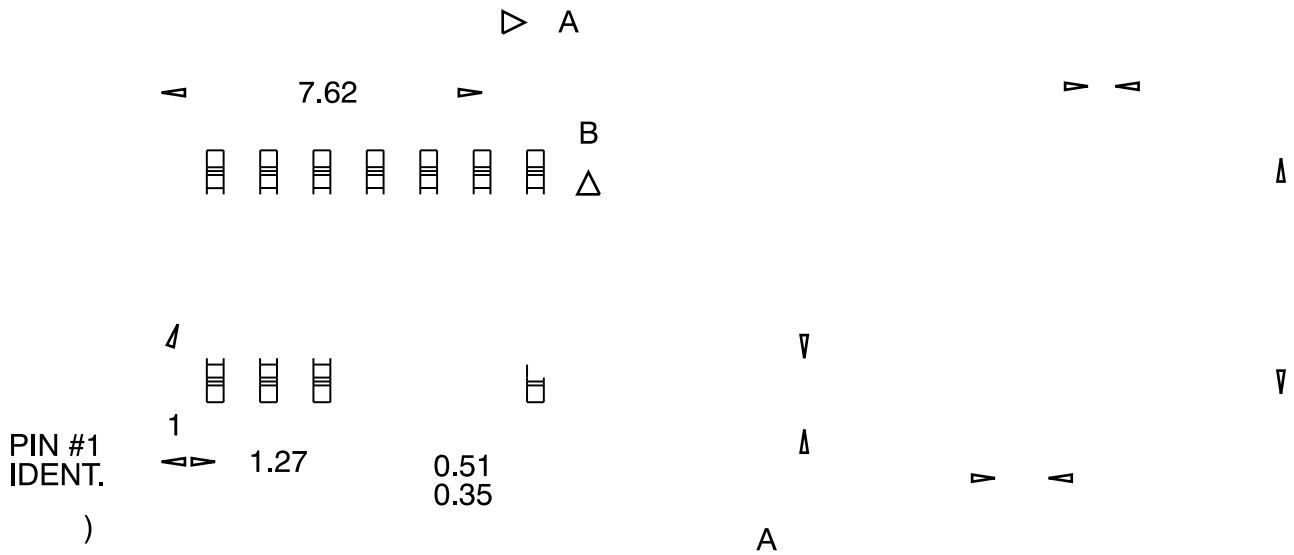
STYLES ON PAGE 2



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STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE

SOIC14



	0.10 (0.004)
	SEATING PLANE

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