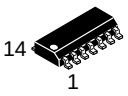
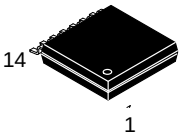
Hex Inverter with Schmitt Trigger Input

74AC14, 74ACT14





The 74AC14 and 74ACT14 contain six inverter gates each with a Schmitt trigger input. They are capable of transforming slowly changing input signals into sharply defined, jitter−free output signals. In addition, they have a greater noise margin than conventional inverters.

The 74AC14 and 74ACT14 have hysteresis between the positive−going and negative−going input thresholds (typically 1.0 V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

- I_{CC} Reduced by 50%
- Outputs Source/Sink 24 mA
- 74ACT14 has TTL−Compatible Inputs
- These are Pb−Free Devices

XXXXXX
AWLYWW

Supply Voltage	V_{CC}	−0.5 to +6.5	V
DC Input Diode Current V_I = −0.5 V V_I = V_{CC} + 1.5 V	I_{IK}	 −20 +20	mA
DC Input Voltage	V_I	−0.5 to V_{CC} + 1.5	V
DC Output Diode Current V_O = −0.5 V V_O = V_{CC} + 0.5 V	I_{OK}	 −20 +20	mA
DC Output Voltage	V_O	−0.5 to V_{CC} + 0.5	V
DC Output Source or Sink Current	I_O	±50	mA
DC V_{CC} or Ground Current per Output Pin	I_{CC} or I_{GND}	±50	mA
Storage Temperature Range	T_{STG}	−65 to +150	°C
Junction Temperature	T_J	140	°C

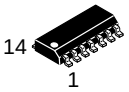
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Publication Order Number:

V_{CC}	Supply Voltage AC ACT			

1.4	V
1.6	
0.4	V
0.5	
2.0	V
2.0	
0.8	V

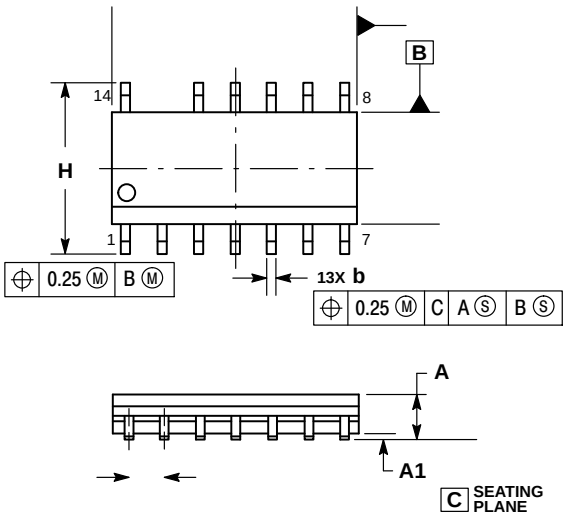
		(Note 6)			



SCALE 1:1

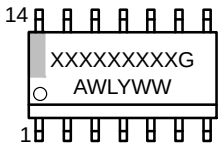
SOIC 14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

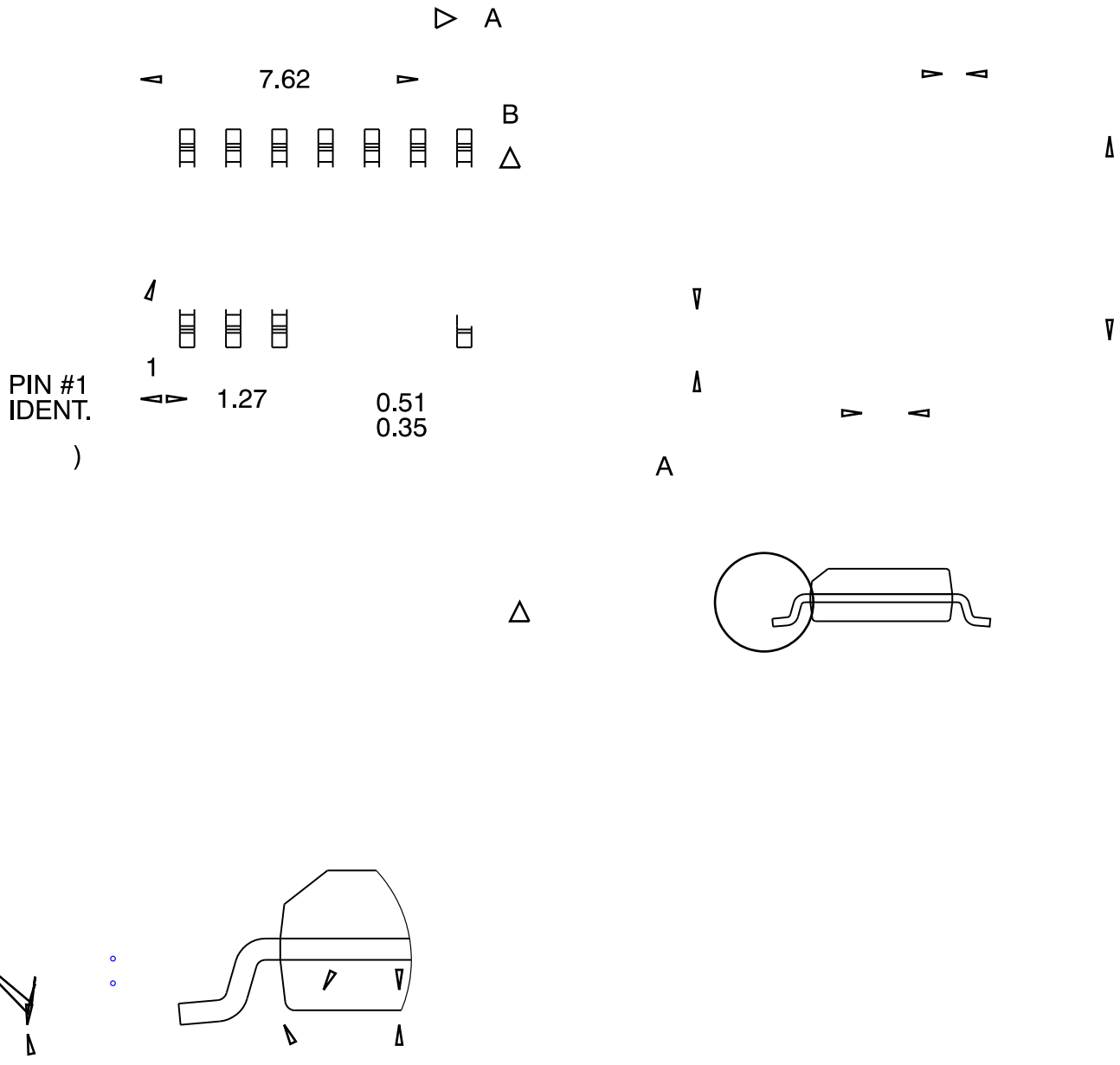
STYLES ON PAGE 2

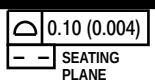
SOIC 14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE

SOIC14




D
0.10 (0.004)
SEATING
PLANE