APPLICATION NOTE
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Key Steps to Design a Compact, High-Efficiency PFC Stage Using NCP1623A

AND90156/D

Description

This paper describes the key steps to rapidly design a CrM/DCM PFC stage driven by the NCP1623. The process is illustrated in a practical 100−W, universal mains application:

- Maximum Output Power: 100 W
- Rms Line Voltage Range: from 90 V to 264 V
- Regulation output voltage:
  - 250 V in low line (115−V mains)
  - 390 V in high line (230−V mains)

Introduction

There’re several options of the NCP1623. This application note focuses on the A version (NCP1623A) which mainly differs from the other versions in the follower boost capability.

Housed in either SOIC−8 or TSOP−6 packages, the NCP1623A is an extremely compact PFC controller

- *Redundant over−voltage protection (OVP2):* CS/ZCD multi−functional pin is used to detect excessive output voltage levels and prevent a destructive output voltage

STEP 1: DEFINE KEY SPECIFICATIONS

- *Line frequency, f_{line}:*

For instance, at low line, full load (top of the sinusoid), the switching frequency is:

$$f_{sw} = \frac{\left(\sqrt{2} \cdot 90\right)^2 \cdot \left(250 - \sqrt{2} \cdot 90\right)}{4 \cdot 105 \cdot 250 \cdot 200 \cdot 10^{-6}} \cong 95\ \text{kHz}$$

STEP 3: IC CONTROL CIRCUIT DESIGN

FB Pin Circuit

As shown by Figure 1, the feed−back arrangement consists of:

- A resistor divider that scales down the bulk voltage to provide the FB pin with the feedback signal. The upper resistor of the divider generally consists of two or three resistors for safety considerations. If not, any accidental shortage of R_{FB1} would apply the output high voltage to the controller and destroy it.
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VCTRL Pin Circuit

In order to find the control to output transfer function, the output voltage is defined by the multiplication of the output current and the output impedance. Using equation 2 and assuming the efficiency is 100%, the output current is given by:

$$i_{out}\left(v_{ctrl},\ v_{out}\right) = \frac{p_{in}}{v_{out}} = \frac{V_{line,rms}{}^{2} \cdot t_{on}}{2 \cdot L \cdot v_{out}}$$

$$= \frac{V_{line,rms}{}^{2} \cdot T_{on.max} \cdot \left(v_{ctrl} - 0.5\right)}{8 \cdot L \cdot v_{out}} \qquad \text{(eq. 33)}$$

The output current partial differentiation by the output voltage is equivalently the output load resistance, R_{load}, based on the equation:

$$\frac{\delta i_{out}}{\delta v_{out}} = -\frac{V_{line,rms}{}^{2} \cdot T_{on.max} \cdot \left(V_{ctrl} - 0.5\right)}{8 \cdot L \cdot v_{out}{}^{2}}$$

$$= -\frac{i_{out}}{v_{out}} = -\frac{1}{R_{load}} \qquad \text{(eq. 34)}$$

Therefore, $\delta i_{out} \ / \ \delta v_{out}$ can be included in the output impedance and total output impedance is:

$$z_{out}(s) = R_{load} \parallel R_{load} \parallel \frac{1}{s \cdot C_{BULK}} \qquad \text{(eq. 35)}$$

The output current partial differentiation by the control voltage is:

δi_{out}

$$R_0 = \frac{390\ \text{V}}{2.5\ \text{V} \cdot 20\ \mu\text{S}} = 780\ \text{k}\Omega$$

$$G_0 = \frac{264\ \text{V}^2 \cdot 5\ \mu\text{s} \cdot 1.52\ \text{k}\Omega}{16 \cdot 200\ \mu\text{H} \cdot 390\ \text{V}} = 424$$

$$C_Z = \frac{424}{2\pi \cdot 25\ \text{Hz} \cdot 780\ \text{k}\Omega} = 3.46\ \mu\text{F} \approx 3.3\ \mu\text{F}$$

$$R_Z = \frac{1.52\ \text{k}\Omega \cdot 68\ \mu\text{F}}{2 \cdot 3.3\ \mu\text{F}} = 15.6\ \text{k}\Omega \approx 15\ \text{k}\Omega$$

$$C_P = \frac{\tan\left(\frac{\pi}{2} - \frac{\pi}{3}\right)}{2\pi \cdot 25\ \text{Hz} \cdot 15\ \text{k}\Omega} = 245\ \text{nF} \approx 220\ \text{pF} \qquad \text{(eq. 46)}$$

CS/ZCD Pin Circuit

The circuit detects an over−current situation if the voltage across the current sense resistor exceeds 0.5 V. Hence:

$$R_{SENSE} = \frac{0.5\ \text{V}}{\left(I_{L,pk}\right)_{max}} \qquad \text{(eq. 47)}$$

Combining the result in equation 6 leads to:

$$R_{SENSE} = \frac{0.5\ \text{V}}{3.3\ \text{A}} = 0.15\ \Omega \qquad \text{(eq. 48)}$$

In our practical case, 0.12 Ω resistor is selected to have a bit of margin. R_{SENSE} losses can be computed using equation 10 giving the MOSFET conduction losses where R_{SENSE} replaces $R_{DS(on)}$:

$$\left(P_{RSENSE}\right)_{max} = \frac{4}{3} \cdot R_{SENSE} \cdot \left(\frac{P_{out,max}}{\eta \cdot \left(V_{line,rms}\right)_{LL}}\right)^2 \cdot \left(1 - \frac{8\sqrt{2} \cdot \left(V_{line,rms}\right)_{LL}}{3\pi \cdot V_{out,LL}}\right) \qquad \text{(eq. 49)}$$

Hence, our 0.12 Ω current sense resistor will dissipate about 124 mW at full load, low line.

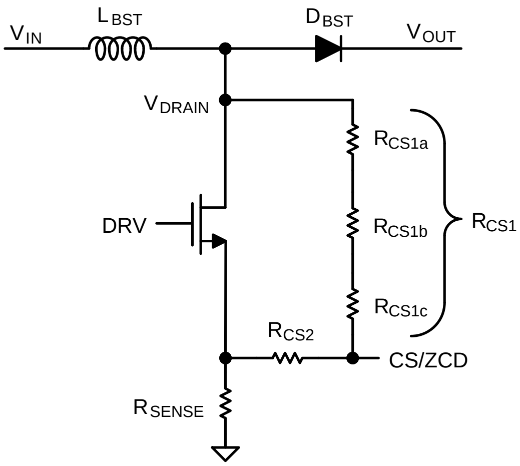

Figure 3. Drain Sensing for ZCD

The drain sensing based ZCD circuitry is shown in Figure 3. Drain voltage is sensed by CS resistor network and scaled down by K_{CS}:

$$K_{CS} = \frac{R_{CS1} + R_{CS2}}{R_{CS2}} \qquad \text{(eq. 50)}$$

where K_{CS} is 133 and R_{CS2} is 62 kΩ in general.

The values of R_{CS1} and R_{CS2}

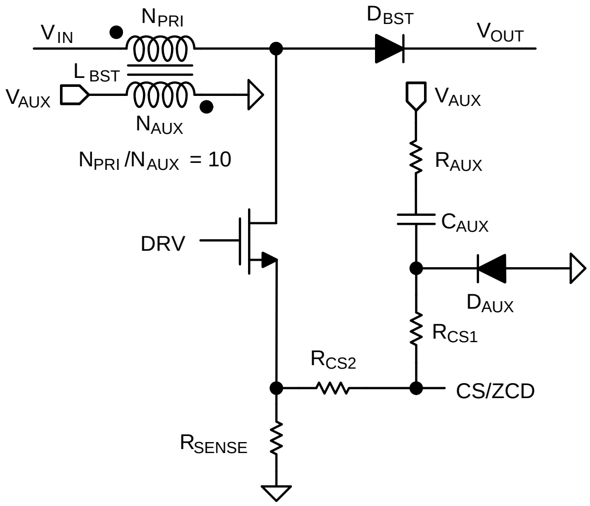

Figure 4. Aux. Winding Sensing for ZCD

It is possible to use the schematic shown in Figure 4 to generate the signal of CS/ZCD pin. Thanks to the auxiliary winding voltage capacitor C_{AUX}, R_{AUX} and D_{AUX}, it is possible to generate at the cathode of D_{AUX} a voltage equal to the power MOSFET drain voltage multiplied by the auxiliary (N_{AUX}) to primary (N_{PRI}) transformer turns ratio. The parameter K_{CS} previously described is now defined by:

$$K_{CS} = \frac{N_{PRI}}{N_{AUX}} \cdot R_{CS1} + R$$

SUMMARY

Table 1. MAIN EQUATIONS

<table>
<tr><th>Step</th><th>Components</th><th>Formula</th><th>Comments</th></tr>
<tr><td>Step 1:
Key Specifications</td><td colspan="3">f_{line}: Line frequency. It is generally specified in a range of 47 − 63 Hz for 50 Hz/60 Hz applications.
$(V_{line,rms})_{HL}$: Lowest Level of the line voltage, e.g., 90 V.
$(V_{line,rms})_{LL}$: Level for the line voltage, e.g., 264 V.
$V_{out,nom}$: Nominal Output Voltage at high−line, e.g., 390 V.
$V_{out,LL}$: Output voltage at low−line (by follower boost) , e.g., 250 V.
$(\delta V_{out})_{pk-pk}$: Peak−to−Peak output voltage ripple in the line frequency
$t_{HOLD-UP}$: Hold−up Time that is the amount of time the output will remain valid during line drop−out, e.g., 10 ms.
$V_{out,min}$: Minimum output voltage allowing for operation of the downstream converter, e.g., 180 V.
$P_{out,max}$: Maximum output power consumed by the PFC load, e.g., 100 W.
η: System efficiency, e.g., 95%.
$(P_{in,avg})_{max}$: Maximum input power from the mains line at full load and low−line, e.g., 105 W assuming η = 95%.</td></tr>
<tr><td rowspan="10">Step 2:
Power Stage Design</td><td rowspan="3">PFC Inductor</td><td>$L \le \dfrac{(V_{line,rms})_{LL}^{2}}{2 \cdot (P_{in,avg})_{max}} \cdot T_{on,max}$</td><td>Maximum inductance
$T_{on,max}$: max turn−on time</td></tr>
<tr><td>$(I_{L,pk})_{max} = 2\sqrt{2}\dfrac{(P_{in,avg})_{max}}{(V_{line,rms})_{LL}}$</td><td>Maximum peak current</td></tr>
<tr><td>$(I_{L,rms})_{max} = 2\sqrt{2}\dfrac{(I_{L,pk})_{max}}{\sqrt{6}}$</td><td>Maximum rms current</td></tr>
<tr><td>Bridge Diode</td><td>$(P_{bridge})_{max} \approx \dfrac{1.8 \cdot V_f \cdot P_{out,max}}{(V_{line,rms})_{LL} \cdot \eta}$</td><td>Maximum power loss
V_f: bridge diode forward voltage</td></tr>
<tr><td>MOSFET</td><td>$(P_{on})_{max} = \dfrac{4}{3} \cdot R_{DS(on)} \cdot \left(\dfrac{P_{out,max}}{\eta \cdot (V_{line,rms})_{LL}}\right)^{2} \cdot \left(1 - \dfrac{8\sqrt{2} \cdot (V_{line,rms})_{LL}}{3\pi \cdot V_{out,LL}}\right)$</td><td>Maximum conduction loss
$R_{DS(on)}$: FET on−state resistance</td></tr>
<tr><td>Boost Diode</td><td>$(P_{diode})_{max} = V_f \cdot \dfrac{P_{out,max}}{V_{out,LL}}$</td><td>Maximum conduction loss</td></tr>
<tr><td rowspan="3">Bulk Capacitor</td><td>$C_{BULK} \ge \dfrac{P_{out,max}}{(\delta V_{out})_{pk-pk} \cdot \omega \cdot V_{out,LL}}$</td><td>Minimum capacitance
to meet output ripple spec</td></tr>
<tr><td>$C_{BULK} \ge \dfrac{2 \cdot P_{out,max} \cdot t_{HOLD-UP}}{V_{out,LL}^{2} - V_{out,min}^{2}}$</td><td>Minimum capacitance
to meet hold−up time spec</td></tr>
<tr><td>$(I_{c,rms})_{max} \cong \sqrt{\dfrac{32\sqrt{2}}{9\pi} \cdot \dfrac{(P_{in,avg})_{max}^{2}}{(V_{line,rms})_{LL} \cdot V_{out,LL}} - \left(\dfrac{P_{out,max}}{V_{out,LL}}\right)^{2}}$</td><td>Maximum rms current</td></tr>
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Table 1. MAIN EQUATIONS (continued)

Step	Comments

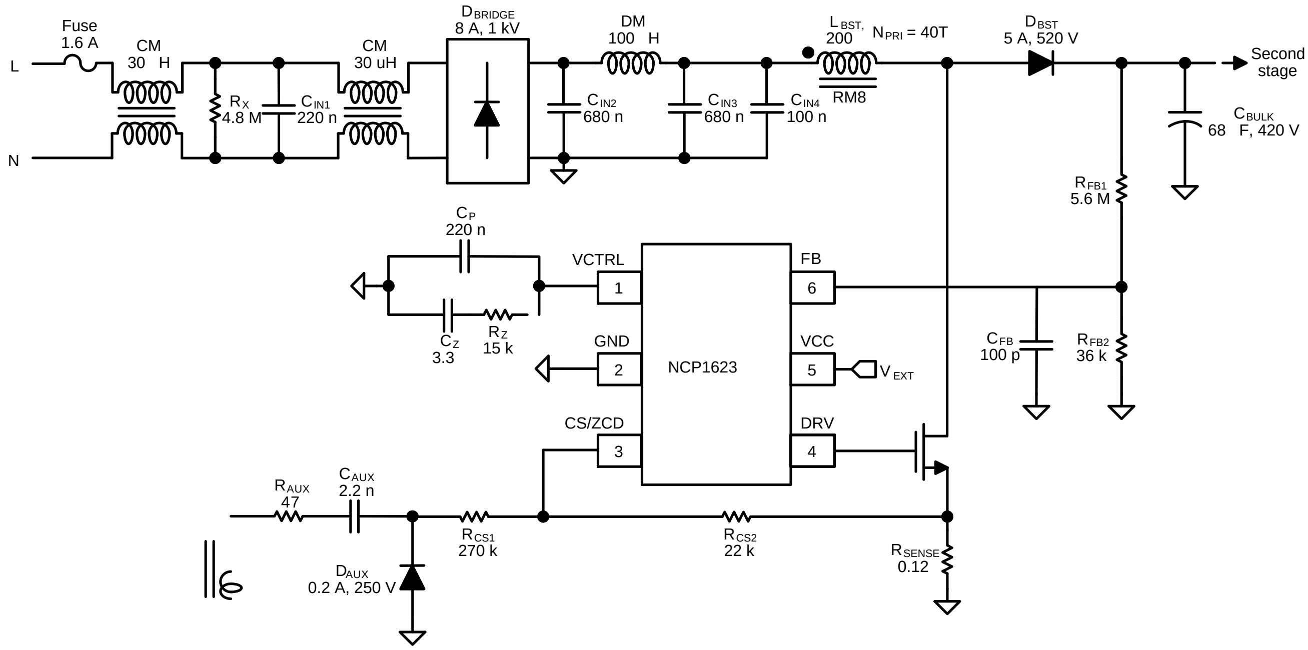

Figure 5. System Schematic of 100 W Design